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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/737,606	12/14/2000	Pierre Leroux		8081

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EXAMINER	
PAREKH, NITIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/737,606	LEROUX, PIERRE	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03-09-01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 7 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamamura (US Pat. 5250983- see IDS).

Regarding claims 1, 2 and 7, Yamamura discloses wafer (see wafer pattern in Fig. 6) for fabricating integrated circuits (IC) using a stepper, the wafer comprising:

- a first region of the wafer (see right side region of 60a in Fig. 6), the first region having four sides and having a scribe line (see scribe line regions in the peripheral area in Fig. 6; shown as 44 in Fig. 4) along each of the four sides of the first region
- four alignment targets disposed within the scribe line at each mid-point of respective side of the first region (not numerically referenced- see alignment patterns on each side in Fig. 6; similar to 46a-46d of the reticle in Fig. 4), the opposing sides of the first region being equal in length (see Fig. 6)
- the alignment targets comprising a plurality of rectangles (see Fig. 6)
- wherein one alignment target is located on each of the four sides of the first region, wherein a first alignment target on a first side of the first region and a

second alignment target on a second side of the first region opposing said first side are located in mirror-image positions (see the left and right alignment patterns opposing on the vertical sides on the first region/right side region of 60a respectively in Fig. 6), and wherein the second alignment target has a width (see the width of second alignment target shown at 62a in Fig. 6) that corresponds to a stepper rotational error between the first region and an adjacent second region of the wafer (see Col. 4, lines 10-22)

(Fig. 6; Col. 4, lines 7-22; Fig. 4-6; Col. 2-4; Col. 2, line 45- Col. 4, line 30).

Regarding claim 21, Yamamura discloses the entire claimed structure as applied to claim 1 above, wherein Yamamura discloses the alignment target being disposed in a first scribe line (see the alignment target of the first region in 62a in Fig. 6) which is in a common region (see 62a in Fig. 6) between a first stepper shot and a second stepper shot (Col. 4, lines 10-22).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamura (US Pat. 5250983- see IDS) in view of Lin (US Pat. 6071656-see IDS).

Regarding claim 3, Yamamura teaches the entire claimed structure as applied to claim 1 above, except the alignment target being located at each corner of the first region.

Lin teaches using conventional alignment marks (206 in Fig. 3) located at each corner of scribe line area of a region on a chip (Col. 3).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the alignment target being located at each corner of the first region as taught by Lin so that the desired alignment accuracy can be achieved in Yamamura's wafer.

5. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamura (US Pat. 5250983- see IDS) in view of Wolf et al. (See "Silicon Processing for the VLSI era"; Vol. 1, 1986, pp.478).

Regarding claims 4 and 5, Yamamura teaches the entire claimed structure as applied to claim 1 above, except the alignment targets being formed according to a positive or a negative resist process.

Wolf et al. teach forming conventional positive or negative images/patterns corresponding to transparent or opaque fields (see Fig. 21, pp. 478).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the alignment targets being formed according to a positive or a negative resist process as taught by Wolf et al. so that the desired process/equipment flexibility can be achieved in Yamamura's wafer fabrication.

Response to Arguments

6. Applicant's arguments with respect to claims 1-4, 7 and 21 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Steven Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

09-03-05

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800